IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A method for fabricating an electronic component with a self-aligned source, drain and gate, comprising the steps of:

a) forming a dummy gate on a silicon substrate, said dummy gate defining a position for a channel of the component;

b) at least one implantation of doping impurities in the substrate, to form a source and a drain on either side of the channel, using the dummy gate as an implanting mask;

c) forming a metal layer on the source, drain and dummy gate;

~~c)~~ d) superficial, self-aligned siliciding of the source and drain by selectively siliciding the metal layer on the source and drain;

~~d)~~ e) depositing at least one contact metal layer having a total thickness greater than a height of the dummy gate, polishing the at least one contact metal layer stopping at the dummy gate, and ~~realizing a surface insulation~~ imparting an insulation characteristic to a surface region of the at least one contact metal layer and the metal layer on sides of the gate electrode; and

~~e)~~ f) replacing the dummy gate by at least one final gate separated from the substrate by a gate insulating layer, and electrically insulated from the source and drain.

Claim 2 (Currently Amended): The method according to claim 1, wherein step ~~d)~~ e) comprises depositing a first metal layer and, above the first metal layer, a second metal layer having a greater mechanical resistance to polishing than the first metal layer, a thickness of the first metal layer being less than the height of the dummy gate, and a total thickness of the first and second metal layers being greater than the height of the dummy gate.

Claim 3 (Previously Presented): The method according to claim 1, further comprising, before siliciding, forming side spacers on sides of the dummy gate.

Claim 4 (Currently Amended): The method according to claim 3, wherein ~~dual-layer~~ the side spacers are formed comprising an attachment layer in silicon oxide, in contact with the dummy gate, and a superficial layer in silicon nitride.

Claim 5 (Previously Presented): The method according to claim 2, wherein a metal of the first metal layer is chosen from among tungsten and titanium, and a metal of the second metal layer is chosen from among TaN, Ta and TiN.

Claim 6 (Previously Presented): The method according to claim 1, wherein the surface insulation comprises superficially oxidizing the at least one contact metal layer.

Claim 7 (Previously Presented): The method according to claim 1, wherein the silicon substrate comprises a solid substrate.

Claim 8 (Previously Presented): The method according to claim 1, wherein the silicon substrate comprises a silicon on insulator substrate.

Claim 9 (Currently Amended): The method according to claim 1, wherein step ~~e)~~ f) comprises removing the dummy gate, forming the gate insulating layer, depositing at least one metal layer to form the final gate, having an overall thickness equal to or greater than the height of the removed dummy gate.

Claim 10 (Previously Presented): The method according to claim 9, further comprising, after forming the gate insulating layer, depositing a first gate metal layer, depositing at least one inter-gate dielectric layer, and depositing a second gate metal layer.

Claim 11 (Previously Presented): The method according to claim 1, wherein the surface insulation comprises depositing a layer of dielectric material.